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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,237	03/04/2002	Dawei Huang	HUANG 3 (58661)	6580

7590 12/13/2005

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,237	HUANG, DAWEI	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 09/27/2005 has been entered. Claims 1-23 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see Remarks of the Amendment, filed on 09/27/2005, with respect to the rejection(s) of claim(s) 1-11 and 13-22 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Alamouti U.S. Patent 5,931,965, Kato et al. U.S. Patent 5,436,918 and Shimoda U.S. Patent 6,122,120.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alamouti U.S. Patent 5,931,965 in view of Kato et al. U.S. Patent 5,436,918 and Shimoda U.S. Patent 6,122,120.

Regarding claim 1, figure 8 of Alamouti invention illustrates a wireless communication system, which employs cyclic trellis error encoding. In column 22, lines 5-40, Alamouti discusses that in catastrophic codes, a finite sequence of errors in the received signal sequence may result in an indefinite sequence of decoding errors. One sign that a code could result in a catastrophic encoder implementation is that, in a next-state table, a present state transitions into the same next state with a given output, while another present state transitions into the same next state with the same given output. The catastrophic code has distance spectrum containing an infinite component that corresponds to a finite hamming weight as appreciated by one of ordinary skill in the art.

As recited above, the wireless communication system in figure 8 employs cyclic trellis encoder 810 for encoding digital data input.

Alamouti does not teach the claimed limitation "*circuit being operative for periodically inserting known symbols into the digital input data sequence*".

Kato et al. teaches in another US Patent a convolutional error correction encoding apparatus (see figure 4A), wherein a fixed value (0 or 1) of one or a plurality of bits is inserted into the information signal series to be error correction encoded; see column 2 line 55 via column 3 line 10. In view of the foregoing disclosure, fixed bits are periodically inserted into digital input data sequence. In column 7 lines 50-60 of Alamouti invention, Alamouti discusses that Trellis-coded modulation is a forward error correction coding technique, which is also well known in the art. Trellis codes are convolutional codes that are designed and

optimized according to a specific modulation scheme. Alamouti and Kato et al. teachings are in the same field of endeavor because both teachings employ convolutional codes for error correction encoding. Furthermore, because Kato et al. teaches using a fixed known bit position, the state transition corresponding to a fixed bit position is limited to only one kind that is determined by the known value (0 or 1) of the fixed bit (see column 2 line 55 via column 3 line 10); therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that Alamouti teachings can be modified to implement Kato et al. teachings of inserting known symbols of 0 or 1.

Nevertheless, Alamouti and Kato et al. et al. do not teach inserting known symbols into digital data sequence for preventing catastrophic error propagation as set forth in the claim.

In column 1 lines 30-45, Shimoda in another US Patent discusses in the Background of the Invention that a prior art discloses a modified expanded – expanded Partial Response Class 4 can cause a catastrophic code at some encoding rate. One of the solution is to increase of the longest 0 consecutive value to obviate the occurrence of the catastrophic code. Because inserting 0 known symbols would obviate the occurrence of the catastrophic code as discussed in Shimoda invention, and the known symbols make the state transition corresponding to a fixed bit position is limited to only one kind that is determined by the known value (0 or 1) of the fixed bit as taught in Kato et al. invention, it would it would have been obvious for one of ordinary skill in the art at

the time of the invention that Alamouti teachings can be modified to implement Kato et al. teachings of inserting known symbols of 0 to obviate the occurrence of the catastrophic code as taught by Shimoda.

Regarding claim 2, as discussed in claim 1, Kato et al. teaches a convolutional error correction encoding apparatus (see figure 4A), wherein a fixed value (***0*** or 1) of one or a plurality of bits is inserted into the information signal series to be error correction encoded; see column 2 line 55 via column 3 line 10.

Regarding claim 3, as recited in Alamouti invention, trellis-coded modulation is a forward error correction coding technique, which is also well known in the art. Trellis codes are convolutional codes that are designed and optimized according to a specific modulation scheme. In view of that, the Trellis encoder 810 in figure 8 is convolutional encoder.

Regarding claim 4, as recited in claim 1, because Kato et al. teaches using a fixed known bit position, the state transition corresponding to a fixed bit position is limited to only one kind that is determined by the known value (0 or 1) of the fixed bit (see column 2 line 55 via column 3 line 10). In view of that, zeros are inserted into digital input data sequence, the number of connections between Trellis nodes in a Trellis is reduced. The Trellis encoder 810 encodes the expanded data input to produce a channel coded data stream.

Regarding claim 5, referring to Alamouti invention, the convolutional encoder 200 includes shift register memory units 205, 210, 215, as well as summers 220, 225 as shown in figure 2A. Memory units 205, 210, 215 have finite length, e.g. m length, corresponding to the claimed memory length m. Because fixed value (0 or 1) of one or a plurality of bits is inserted into the information signal series to be error correction encoded as taught by Kato et al., the plurality of bits is inserted after each m symbol.

Regarding claim 6, claim 6 is rejected on the same ground as for claim 1 because claim 1 claims a system performing steps in claim 6.

Regarding claim 7, claim 7 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 8, as recited in claim 5, according to Kato et al. teachings, fixed value (0 or 1) of one or a plurality of bits is inserted into the information signal series to be error correction encoded. Because redundant bits are appended in the information signal, for the case of memory length equal to two bit symbol, a 0 is inserted after each of two information bits as claimed in the application claim.

Regarding claim 9, using analogous reasons as in claim 8, redundant bits are added after each symbol for error correction. Hence, for the case of four-bit symbol, one zero can be inserted between every four bits of data points.

Regarding claims 10 and 13, claims 10 and 13 are rejected on the same ground as for claim 3 because of similar scope.

Regarding claim 11, because zeros are inserted between information bits. Convolutional code includes time varying convolutional code.

Regarding claim 12, Kato et al. teaches using a fixed known bit position, the state transition corresponding to a fixed bit position is *limited to only one kind that is determined by the known value* (0 or 1) of the fixed bit (see column 2 line 55 via column 3 line 10). Therefore, the convolutional code including inserted values of 0, corresponding to the claimed nonzero input sequence corresponds to an all-zero output sequence.

Regarding claim 14, claim 14 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 15, claim 15 is rejected on the same ground as for claim 4 because of similar scope.

Regarding claim 16, claim 16 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 17, for each binary input sequence to trellis diagram, there is one corresponding code word via distinct paths. Therefore, application of code word is one-to-one mappings to binary input sequence.

Regarding claim 18, claim 18 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 19, claim 19 is rejected on the same ground as for claim 8 because of similar scope.

Regarding claim 20, claim 20 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 10 because of similar scope.

Regarding claim 22, claim 22 is rejected on the same ground as for claim 11 because of similar scope.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 12 because of similar scope.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh cong Tran 12/09/2005

Examiner KHANH TRAN